

IPalette™

Think  
Envision  
Invent the future

## Graphical Block Diagram Entry and System Definition for HDL-Based Design.

An easy-to-use graphical approach that lets you quickly specify high-level system descriptions as a collection of hierarchically decomposed, functionally partitioned block diagrams.



## Top-down

Now Exsedia's IPalette™ toolset makes it easier and faster for VHDL and Verilog® designers to build high-quality large scale systems. In a top-down approach where there are existing multiple HDL components, IPalette allows you to use block diagrams to structure and partition your design, then add in the internal descriptions using the IPalette code editor and Nimbus™ behavioral descriptions. IPalette gives you structured VHDL or Verilog code—no more headaches tracing errors in connectivity between entity/architectures or modules.

## Bottom-up

IPalette also lets you build systems bottom-up by allowing you to take existing VHDL architecture or Verilog module code blocks and behavioral descriptions created in Nimbus, and bind them to block diagrams which define your system's hierarchy. By binding system-level modules from your components, you can then maximize design reuse.

## IPalette helps you:

- Visualize the hierarchical structure of large, complex systems
- Create structured templates for language-based design
- Produce high-quality design documentation to manage complex HDL design
- Design systems and components that are easy to modify, maintain and reuse
- Bind design components and test harnesses together
- Build correctly structured and connected designs the first time around

## Features

**Notation** In IPalette, graphical entry takes the form of block diagrams. Hierarchically decomposed blocks represent various components of a system. Blocks contain signals that are connected to other blocks through the use of nets. Junction boxes are used to route individual bits of these signals.

**Navigation** IPalette provides several tools to navigate through its hierarchical structure. Mouse movements can be used to quickly “push” into lower levels or “pop” into higher levels of the design. IPalette also provides a hierarchical browser that allows you to choose a block for editing in the IPalette main window, and simultaneously see other views of the design displayed as “mini views.”

**Defining Signals** Signals are defined and modified in definition boxes, activated by clicking on the signals' associated objects. Users can define a name, type (binary, MVL, or enumerated, and width for the signal. IPalette allows users to define enumerated types as well as binary and standard MVL types.

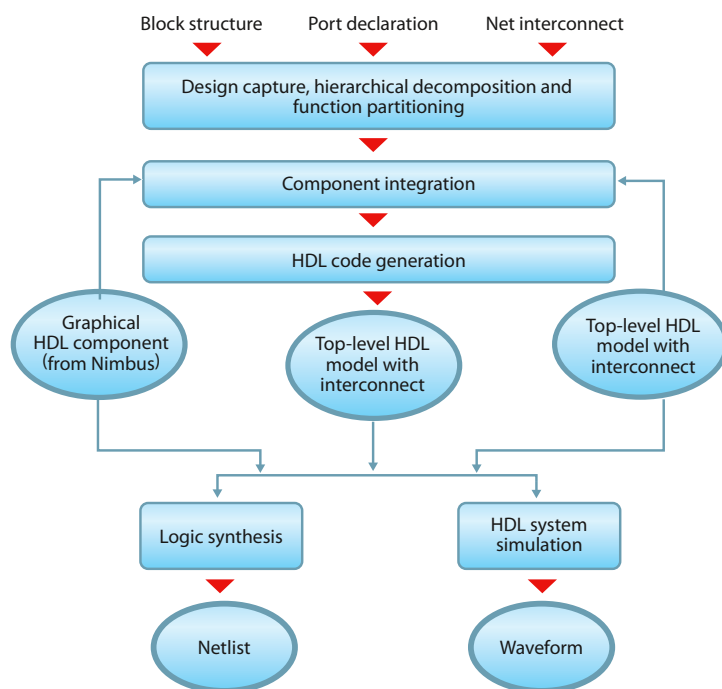
**Text Editor** IPalette contains a text editor for entering and editing VHDL or Verilog code. Text files containing HDL code can also be imported into IPalette from other text editors.

**Binding** The bind feature allows the user to link bottom-level blocks to descriptive elements. Blocks can be bound to a text file, a Nimbus file, another IPalette file, or reinstated as another block within the same design.

**Translation** The design model is translated into VHDL or Verilog code which can be used for your favorite downstream simulation and logic synthesis tools.

**Export** Port declarations in IPalette can be exported to Nimbus, allowing the user to model the behavior of the block and bind it back to Nimbus.

## Functionality and Integration



For more information on IPalette™ and how we can help you, please call, email or fax us at:



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### O/S and System Requirements

Platform supports

- Sun OS 5.7 or Solaris 7.0
- Red Hat 7.2 or 7.3 with Lesstif

### Memory Requirements

- 256MB and 3MB of disk space
- Node-lock and floating licenses available

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